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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,789	12/08/2003	Yuji Amano	L8462.03119	8935

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STEVENS DAVIS MILLER & MOSHER, LLP
1615 L STREET, NW
SUITE 850
WASHINGTON, DC 20036

EXAMINER	
HOANG, ANN THI	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,789	AMANO ET AL.	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6 and 11-14* is/are rejected.

7)☐ Claim(s) *3-4 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because the abstract is too long. Correction is required. See MPEP § 608.01(b) [R-3].

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-6, and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Akihiro (JP 2000-174601).

Regarding claim 1, Akihiro teaches a capacitive load driving circuit (21) for supplying a charging-current (I2) to a capacitive load (CL) and withdrawing a

discharging-current (I1) from said capacitive load (CL), comprising: an output circuit (Q1, Q2, 22, 23) which comprises a power supply terminal (23), a ground terminal, and an output terminal (22) connected to said capacitive load (CL), and which performs a charging-current supplying operation of supplying a charging-current (I2) from said power supply terminal (23) to said capacitive load (CL) and a discharging-current withdrawing operation of withdrawing a discharging-current (I1) from said capacitive load (CL) to said ground terminal; and an overcurrent protection circuit (25-28) for detecting a short circuit between said output terminal (22) and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal (22) and said power supply terminal (23) so as to stop or suppress said discharging-current withdrawing operation; wherein said output circuit (Q1, Q2, 22, 23) selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal (S1). Limiter circuits (27, 28) detect when the voltage of output terminal (22) reaches a predetermined upper voltage limit (E1) or reaches a predetermined lower voltage limit (E2). Akihiro discloses that upper voltage limit (E1) may be set to the voltage of power supply terminal (23) and that lower voltage limit (E2) may be set to the voltage of the ground terminal. If output terminal (22) reaches an upper voltage limit (E1) equal to the voltage of the power supply terminal (23), then there is a short circuit between said output terminal (22) and said power supply terminal (23). If output terminal (22) reaches a lower voltage limit (E2) equal to the voltage of the ground terminal, then there is a short circuit between said output terminal (22) and said

ground terminal. Upon either of these occurrences, control circuits (25, 26) suppress the charging and discharging-currents (I2, I1). See Fig. 1, abstract, and paragraphs 14 and 26.

Regarding claim 2, Akihiro discloses that the output circuit (Q1, Q2, 22, 23) continues to charge said capacitive load (CL) in said charging-current supplying operation until the electrical potential of said capacitive load (CL) reaches a predetermined upper amplitude limit (E1) lower than the electric potential of said power supply terminal (23), and continues to discharge said capacitive load (CL) in said discharging-current withdrawing operation until the electric potential of said capacitive load (CL) reaches a predetermined lower amplitude limit (E2) higher than the electric potential of said ground terminal. As long as the potential of the load capacity (CL) stays within a prescribed upper limit (E1) and lower limit (E2), control circuits (25, 26) will continue to supply base currents (I1, I2) of output transistors (Q1, Q2).

Regarding claim 5, Akihiro discloses the state of said control input signal (S1) as alternating periodically. See Fig. 2, in which (S1) is shown to be a periodic square wave.

Regarding claim 6, all the limitations of claim 6 are recited in claim 1 with the exception of the current generation circuit and the charging and discharging control circuit. Akihiro teaches a current generation circuit (2) for selecting, depending on the state of a control input signal (S1), any one of a first state where a first current (I2) is supplied to said output circuit (Q1, Q2, 22, 23) so as to cause said output circuit (Q1, Q2, 22, 23) to select said charging-current supplying operation and a second state

where a second current (I1) is supplied to said output circuit (Q1, Q2, 22, 23) so as to cause said output circuit (Q1, Q2, 22, 23) to select said discharging-current withdrawing operation; and a charging and discharging control circuit (25-28) for detecting the electric potential of said capacitive load (CL) and thereby controlling and causing said output circuit (Q1, Q2, 22, 23) to continue said charging-current supplying operation until the electric potential of said capacitive load (CL) reaches a predetermined upper amplitude limit (E1), to stop said charging-current supplying operation when said electric potential reaches said predetermined upper amplitude limit (E1), to continue said discharging-current withdrawing operation until the electric potential of said capacitive load (CL) reaches a predetermined lower amplitude limit (E2), and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit (E2). See abstract, Figs. 1 and 4, and paragraph 2.

Regarding claim 11, the acknowledged prior art of Applicant's disclosure teaches frequency-dependent impedance elements (C1, C2) to be provided between said current generation circuit (51) and said output circuit (21), so that a part of the output current of said output circuit (21) is fed back through said frequency-dependent impedance elements (C1, C2) to said current generation circuit (51), so that the through-rate is suppressed at the alternation of the output state of said current generation circuit (51). See Figs. 3-4 and page 38, lines 11-20.

Regarding claim 12, Akihiro discloses the state of said control input signal (S1) as alternating periodically. See Fig. 2, in which (S1) is shown to be a periodic square wave.

Regarding claim 13, all the limitations of claim 13 are recited in claim 1 except that, instead of the output terminal being connected to a general capacitive load as in claim 1, the output terminal in claim 13 is connected to a liquid crystal display panel common electrode. Akihiro teaches the output terminal as being characterized by the common electrode of a liquid crystal display panel. See paragraph 21.

Regarding claim 14, all the limitations of claim 14 are recited in claim 6 except that, instead of the output terminal being connected to a general capacitive load as in claim 6, the output terminal in claim 14 is connected to a liquid crystal display panel common electrode. Akihiro teaches the output terminal as being characterized by the common electrode of a liquid crystal display panel. See paragraph 21.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 5-6, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art in view of Stodolsky (US 3,550,025).

Regarding claim 1, the acknowledged prior art of Applicant's disclosure teaches a capacitive load driving circuit (Fig. 3) for supplying a charging current (I2) to a capacitive load (CL) and withdrawing a discharging-current (I7) from said capacitive load (CL), comprising: an output circuit (21) which comprises a power supply terminal (17), a ground terminal (18), and an output terminal (16) connected to said capacitive

load (CL), and which performs a charging-current supplying operation of supplying a charging-current (I2) from said power supply terminal (17) to said capacitive load (CL) and a discharging-current withdrawing operation of withdrawing a discharging-current (I7) from said capacitive load (CL) to said ground terminal (18); and wherein said output circuit (21) selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal (S1). The acknowledged prior art does not teach an overcurrent protection circuit for detecting a short circuit between said output terminal (16) and said ground terminal (18) or said power supply terminal (17) so as to stop or suppress said charging-current supplying operation or said discharging-current withdrawing operation.

However, Stodolsky discloses an overcurrent protection circuit (11, 12, 33, 34) for detecting a short circuit between an output terminal (D) and a ground terminal so as to stop or suppress a charging-current supplying operation, and for detecting a short circuit between said output terminal (D) and a power supply terminal so as to stop or suppress a discharging-current withdrawing operation. Output terminal D is disclosed as possibly being connected to a capacitive load. See column 2, lines 53-55. The load is charged through positive cycle driver (11) and positive cycle analog gate (13) and discharged by negative cycle driver (12) and negative cycle analog gate (14). See Fig. 1 and column 3, lines 33-37. In Fig. 2, the comparator, and gates, and analog gates (13, 14) of Fig. 1 are consolidated into positive and negative cycle logic blocks (33, 34), the analog gates (13, 14) of Fig. 1 being represented here by PNP transistor (35) and NPN transistor (36). If the comparator and logic controls sense output (D) as being

shorted to ground, the complement transistor (35) is shut off to cease the charging of the load. Similarly, if output (D) is shorted to the power supply, transistor (36) is shut off to cease the discharging of the load. Thus, overcurrent destruction is prevented for each output transistor (35, 36) upon the occurrence of a collector-emitter breakdown in its complement output transistor. See column 2, lines 41-42 and 56-72 and column 3, lines 1-4. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the overcurrent protection circuit of Stodolsky in the capacitive load driving circuit of the acknowledged prior art in order to prevent overcurrent destruction to each output transistor upon its complement being shorted.

Regarding claim 2, the acknowledged prior art of Applicant's disclosure teaches that said output circuit (21) continues to charge said capacitive load (CL) in said charging-current supplying operation until the electric potential of said capacitive load (CL) reaches an upper amplitude limit, and continues to discharge said capacitive load (CL) in said discharging-current withdrawing operation until the electric potential of said capacitive load (CL) reaches a lower amplitude limit. See page 2, lines 9-14. The upper limit would necessarily be a predetermined upper amplitude limit lower than the electric potential of said power supply terminal and the lower limit would necessarily be a predetermined lower amplitude limit higher than the electric potential of said ground terminal in order to establish an acceptable voltage range for the output, voltages outside of which constitute a potential too high or too low to continue charging or discharging of the load.

Regarding claim 5, the acknowledged prior art of Applicant's disclosure teaches the state of said control input signal to alternate periodically. See page 2, lines 5-9.

Regarding claim 6, all the limitations of claim 6 are recited in claim 1, rejected above, with the exception of the current generation circuit and the charging and discharging control circuit. The acknowledged prior art of Applicant's disclosure teaches a current generation circuit (51) for selecting, depending on the state of a control input signal (S1), any one of a first state where a first current (I2) is supplied to said output circuit (21) so as to cause said output circuit (21) to select said charging-current supplying operation and a second state where a second current (I7) is supplied to said output circuit (21) so as to cause said output circuit (21) to select said discharging-current withdrawing operation; and a charging and discharging control circuit (22) for detecting the electric potential of said capacitive load (CL) and thereby controlling and causing said output circuit (21) to continue said charging-current supplying operation until the electric potential of said capacitive load (CL) reaches a predetermined upper amplitude limit (V2), to stop said charging-current supplying operation when said electric potential reaches said predetermined upper amplitude limit (V2), to continue said discharging-current withdrawing operation until the electric potential of said capacitive load (CL) reaches a predetermined lower amplitude limit (V1), and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit (V1). See Figs. 3 and 5.

Regarding claim 11, the acknowledged prior art of Applicant's disclosure teaches frequency-dependent impedance elements (C1, C2) to be provided between said

current generation circuit (51) and said output circuit (21), so that a part of the output current of said output circuit (21) is fed back through said frequency-dependent impedance elements (C1, C2) to said current generation circuit (51), so that the through-rate is suppressed at the alternation of the output state of said current generation circuit (51). See Figs. 3-4 and page 38, lines 11-20.

Regarding claim 12, the acknowledged prior art of Applicant's disclosure teaches the state of said control input signal to alternate periodically. See page 2, lines 5-9.

Regarding claim 13, all the limitations of claim 13 are recited in claim 1, rejected above, except that, instead of the output terminal being connected to a general capacitive load as in claim 1, the output terminal in claim 13 is connected to a liquid crystal display panel common electrode. The acknowledged prior art of Applicant's disclosure suggests that it is a known practice to use a capacitive load driving circuit for driving a capacitive load composed of a common electrode of a liquid crystal display panel. See page 1, lines 14-16. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the capacitive load driving circuit as rejected in claim 1 to drive a common electrode of a liquid crystal display panel in order to effectively drive the liquid crystal display without having to build another driving device for the liquid crystal display.

Regarding claim 14, all the limitations of claim 14 are recited in claim 6, rejected above, except that, instead of the output terminal being connected to a general capacitive load as in claim 6, the output terminal in claim 14 is connected to a liquid crystal display panel common electrode. The acknowledged prior art of Applicant's

disclosure suggests that it is a known practice to use a capacitive load driving circuit for driving a capacitive load composed of a common electrode of a liquid crystal display panel. See page 1, lines 14-16. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the capacitive load driving circuit as rejected in claim 1 to drive a common electrode of a liquid crystal display panel in order to effectively drive the liquid crystal display without having to build another driving device for the liquid crystal display.

Allowable Subject Matter

7. Claims 3-4 and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to teach an overcurrent protection circuit comprising a second NPN transistor connected to a first NPN transistor, output terminal, and voltage supply in the manner as specified in the claims, and a second PNP transistor connected to a first PNP transistor, output terminal, and voltage supply in the manner as as specified in the claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ivanov et al. (US 6,807,040) discloses an arrangement of two pairs of PNP BJTs connected such that the collector of the detecting transistor is tied to the base of the

current supplying transistor, the collector of the current supplying transistor is tied to a power supply, and the emitters of both transistors are tied directly or indirectly to an output node. The detecting transistor limits the current through the current supplying transistor if the voltage across a resistor at the emitter of the current supplying transistor exceeds the base emitter voltage of the detection transistor.

Wada et al. (JP 60-13559) discloses a drive circuit for a capacitive load with overcurrent prevention comprising two detection transistors and two current supplying transistors which are connected at their emitters to an output. The detection means senses a current exceeding a predetermined value and controls an opening and closing action of a switch on the basis of the detection signal.

Okutsu et al. (US 4,733,106) discloses a capacitive load driving device comprising a first switching element for supplying a charging current to the load and a second switching element for withdrawing a discharging current from the load. The switching elements are responsive to an external control signal and control circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Monday through Friday, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ATH

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800